Customer No.: 31561
Docket No.: 12447-US-PA
Application No.: 10/708,489

REMARKS

This is a full and timely response to the outstanding final Office Action mailed June 15, 2006. Applicants submit that claim 1 has been amended hereby. There is no new matter entered and thus no new ground can be necessitated. Reconsideration and allowance of the application and presently pending claims 1-6 are respectfully requested.

Claim Rejections – 35 U.S.C. § 102

The Office Action rejected claims 1 and 5-6 under 35 U.S.C. 102(b) as being anticipated by Ooishi US 5,689,460.

In response to the rejection to claims 1 and 5-6 under 35 U.S.C. 102(b) as being anticipated by Ooishi, Applicants amended claim1 and hereby otherwise traverse this rejection. As such, Applicant submits that claims 1, 5 and 6 are now in condition for allowance.

Applicants respectfully traverse the rejections of Claims 1 and 5-6 under 35 U.S.C. 102(b) because Ooishi does not teach every recitation of these claims. For example, Ooishi does not disclose a voltage regulator apparatus having "a first transistor having ...***a third terminal directly coupled to the output terminal of the voltage regulator***" as recited in Claim 1 (emphasis added).

In order to properly anticipate Applicant's claimed invention under 102, each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Further, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." See MPEP §2131, quoting Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Finally, "[t]he elements must be arranged as required by the claim." See MPEP § 2131.

Ooishi's FIG. 11 schematically shows a structure of an internal power supply voltage generation circuit. The circuit includes a comparison circuit 3 for comparing an internal power supply voltage VCI (being an output voltage) on an internal power supply line 5 with a reference voltage Vref, an NMOS transistor N3 connected between an external power supply node 1 and an output node 6 of comparison circuit 3, a PMOS transistor P3 connected between node 6 and a ground node, and a drive transistor 2 for supplying current from external power supply node 1 to internal power supply line 5 according to the voltage on node 6.

Although the circuit disclosed by Ooishi uses the MOS transistors N3 to suppress lowering of the voltage of node 6 and uses the MOS transistor P3 to suppress the voltage rise at node 6, the source terminals of the MOS transistors N3 and P3 are not directly coupled to the output (node 5) of the circuit . As described by Ooishi, the source terminals of the MOS transistors N3 and P3 are coupled to the node 6 and further the node 6 is coupled to the gate

terminal of the drive circuit 2 which outputs the output voltage VCI from its source terminal 5. Thus, in Ooishi's circuit, the source terminals of the MOS transistors N3 and P3 are not directly coupled to the output voltage VCI. Instead, in Ooishi's circuit, the source terminals of the MOS transistors N3 and P3 are directly coupled to the gate terminal of the drive transistor 2 and the output voltage VCI is provided from the source terminal of the drive transistor 2.

Accordingly, Ooishi does not disclose a voltage regulator apparatus having "a first transistor having ...a third terminal directly coupled to the output terminal of the voltage regulator" as recited in Claim 1.

Further, in Ooishi circuit, the drive transistor 2 is necessary because it supplies current to the internal power supply line 5 from the external power supply node 1 according to the output signal of the comparison circuit 3. However, in Claim 1 of the application, no drive transistor for supplying current to the output node is recited.

Because Ooishi does not teach each and every recitation of claim 1, Applicants request that the rejection of this claim under 35 U.S.C. 102(a) be withdrawn and the claim allowed.

Claims 5-6 depend from claim 1. As explained, claim 1 is distinguishable from the cited art. Accordingly, claims 5-6 are also distinguishable from this reference for at least the same

reasons set forth in connection with base claim 1. Further, this reference fails to teach or suggest the recitations of claims 5-6.

Accordingly, because Ooishi fails to teach all of the recitations of claims 5-6, Applicants respectfully request that the Examiner withdraw the rejection of these claims under 35 U.S.C. 102(a) and allow the claims.

Claim Rejections – 35 U.S.C. § 103

The Office Action rejected claims 2-4 under 35 U.S.C. 103(a) as being unpatentable over Ooishi in view of the acknowledged prior art (APA).

Applicant respectfully traverses the rejections of claims 2-4 under 35 U.S.C § 103(a) as being unpatentable over Ooishi in view of APA. To establish a prima facie case of obviousness under 35 U.S.C § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make

the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. See MPEP § 2143.

The Examiner failed to establish prima facie obviousness in rejecting Claims 2-4 because Ooishi and APA, taken alone or combined, fail to teach or suggest, among other things, a voltage regulator apparatus having "a first transistor having ...a third terminal directly coupled to the output terminal of the voltage regulator..." as recited in Claim 1 which claims 2-4 depend from.

The Examiner concedes that Ooishi fails to disclose an error amplifier connected to the structure recited in claim 1. To make up for this deficiency, the Examiner relies on APA to teach these features. Applicant respectfully disagrees with the Examiner's interpretation of the cited art and its application to claim 2.

Even if the cited arts would be combined, which Applicants respectfully disagree, the combination would not have rendered claims 2-4 obvious. In Claim 2 of the application, the recited voltage regulator includes an error amplifier (i.e. a comparator), a third transistor (whose gate terminal being coupled to the output of the comparator) and a load circuit (for diving the output voltage). Ooishi's Fig. 11 and APA show the similar features with each other, i.e. the comparator, the drive transistor and the load circuit. Applicants respectfully submit that there is no motivation to combine two references with much similar or substantially the same features

because the combination of Ooishi and APA still leads a circuit similar or the same as the circuit in Ooishi's Fig. 11 or APA, which means the combination would not have any useful meaning.

Additionally, prima facie obviousness has not been established at least because the requisite motivation to combine Ooishi and APA is lacking. Determinations of obviousness must be supported by evidence in the record. See In re Zurko, 258 F.3d 1379, 1386 (Fed. Cir. 2001) (finding that the factual determinations central to the issue of patentability, including conclusions of obviousness by the Board, must be supported by "substantial evidence"). Further, the desire to combine references must be proved with "substantial evidence" that is a result of a "thorough and searching" factual inquiry. In re Lee, 277 F.3d 1338, 1343-1344 (Fed. Cir. 2002) (quoting McGinley v. Franklin Sports, Inc:, 262 F.3d 1339, 1351-52).

In this case, the Examiner asserts APA provides the requisite motivation because APA discloses "an error amplifier, a third transistor, and a load circuit." (OA at page 3.) This statement does not show a motivation for combining the cited arts. Instead, the Examiner merely recites a feature performed by APA, and does not show how one of ordinary skill in the art would have been motivated to implement these features in the circuit disclosed by Ooishi. The mere fact that APA discloses an error amplifier and Ooishi discloses an internal power supply voltage generation does not show that a skilled artisan would have been motivated to modify the cited arts as alleged.

Therefore, Applicants respectfully submit that there is no motivation to combine the three references, that there is no reasonable expectation of success, and that the references do not teach the elements of the claim. There is no suggestion or motivation in the prior art to make the claimed combination, and no suggestion that, if made, the combination would be successful to achieve the highly useful result that was achieved, for the first time, by the inventors.

The claimed invention was oversimplified by the Examiner, leading the Examiner to combine, in perfect hindsight, Ooishi and APA. No reference contains any motivation or suggestion to combine these teachings; that comes only from hindsight using the claimed invention as the template.

For at least these reasons, the Examiner has not established a prima facie case of obviousness with respect to claims 2-4. Thus, because the cited arts do not support the rejections of claim 2-4 under 35 U.S.C. 103(a), Applicant requests that the rejections be withdrawn and the claims allowed.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-6 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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